

FIGURE 1
(PRIOR ART)

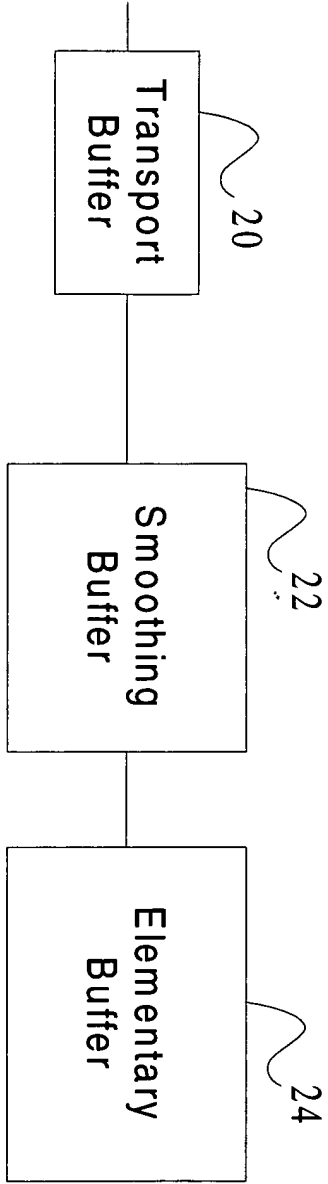
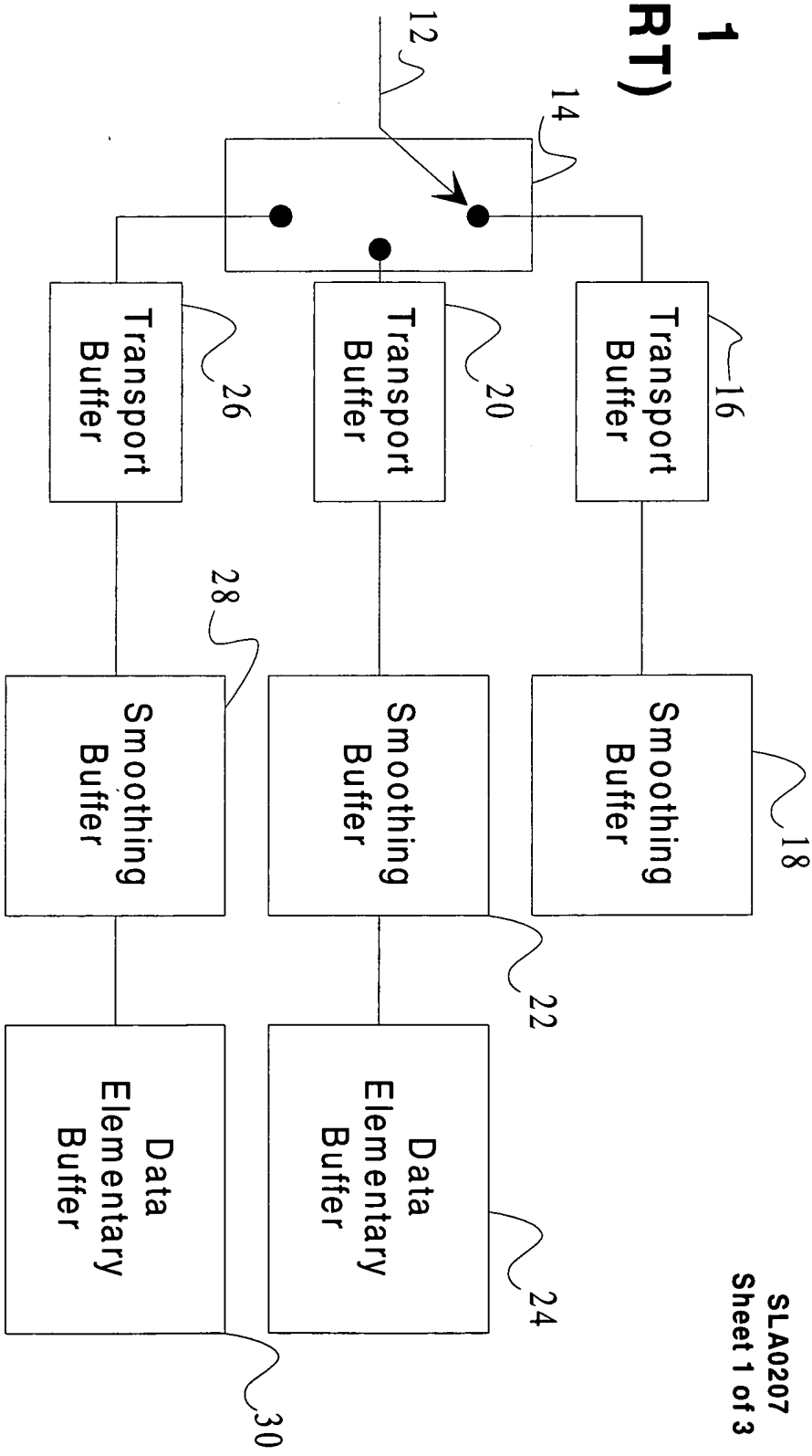


FIGURE 2
(PRIOR ART)

FIGURE 2 is a block diagram of a proposed system. It shows a single processing path. A Transport Buffer 20 is connected to a Smoothing Buffer 22, which is then connected to an Elementary Buffer 24.

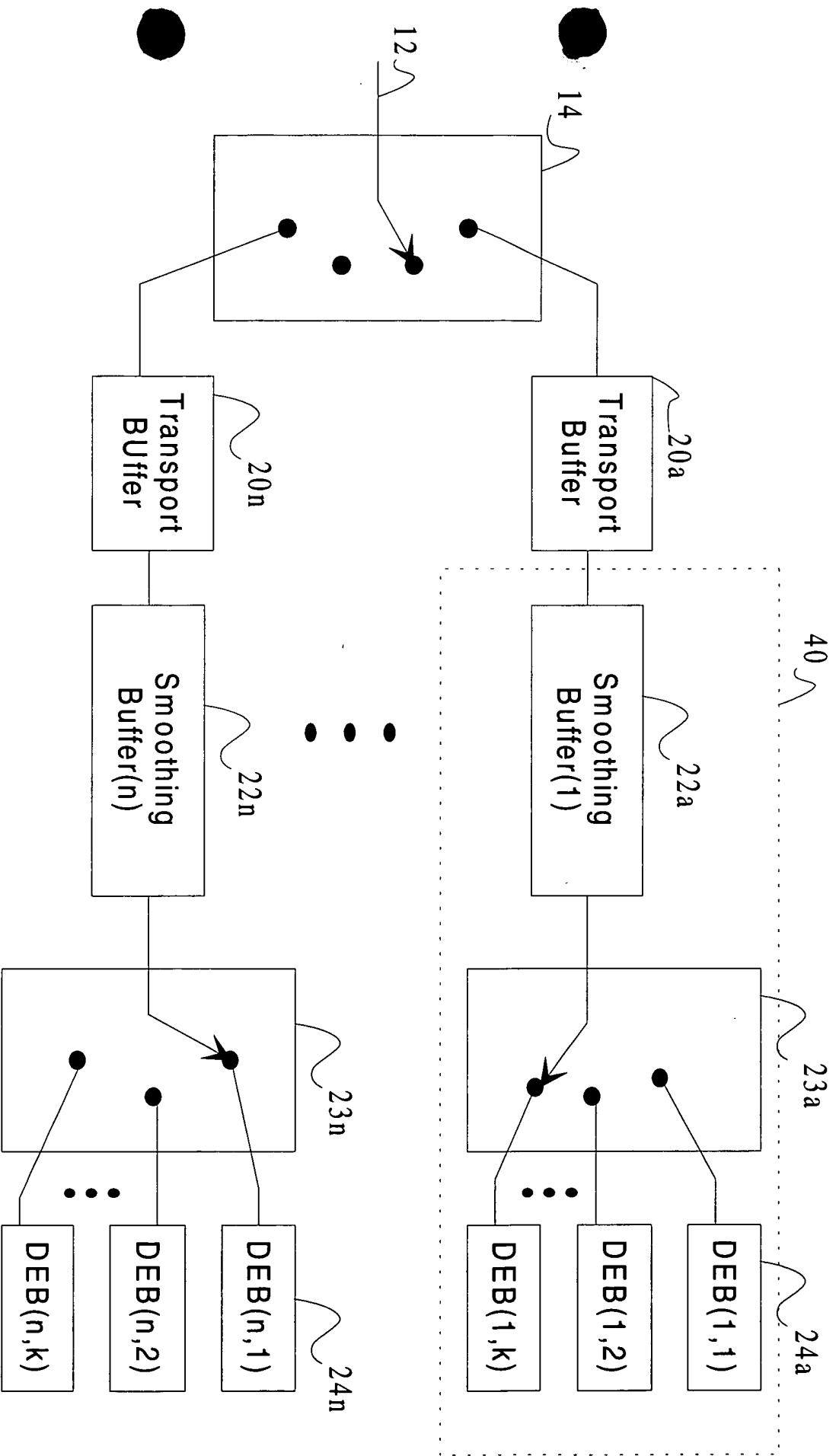


FIGURE 3

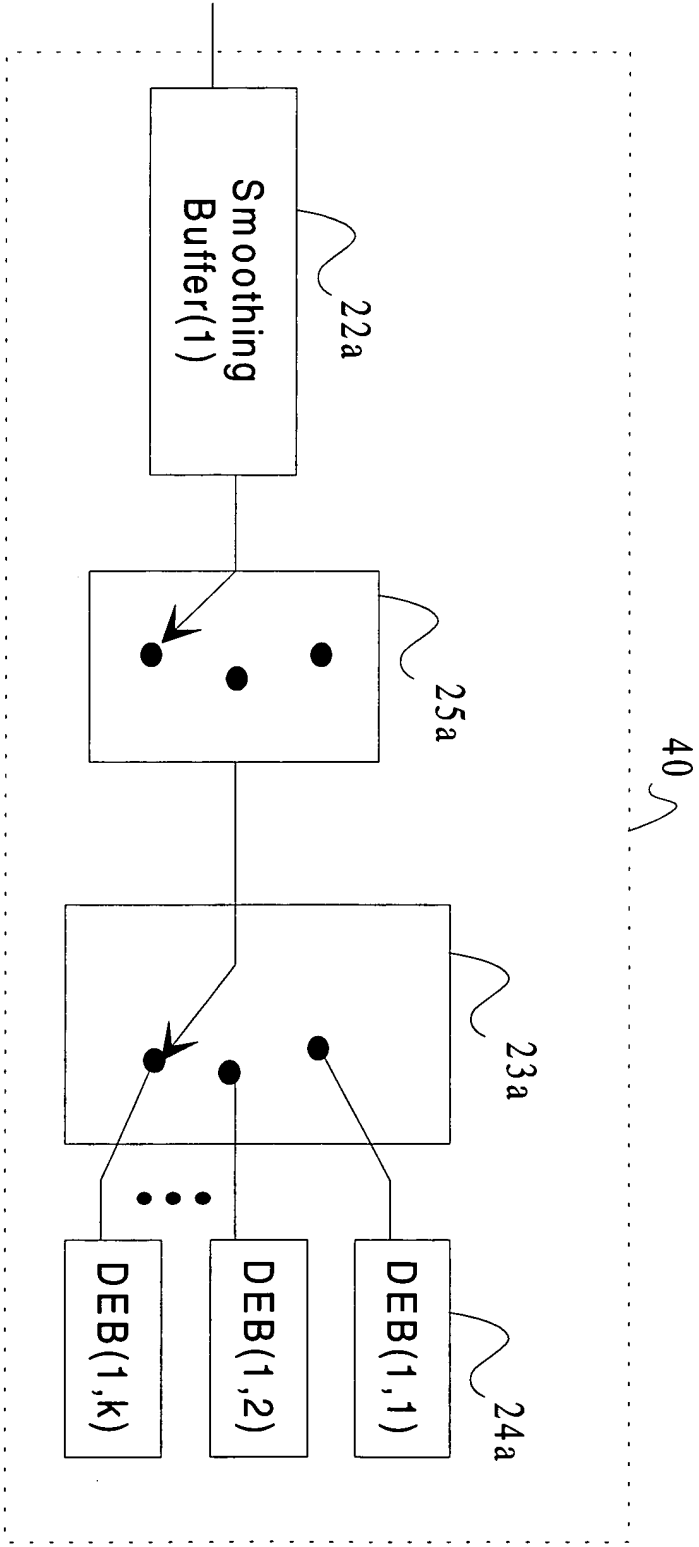


FIGURE 4